

Fractional-N Phase-Locked Loop Surface Mount Module

Applications

- Fixed Wireless
- Test Equipments
-

Application Notes

- AN-107: Manual Soldering Technique
- AN-202: Programming Z-COMM PLLs

Performance Specifications	Min	Typ	Max	Units
Frequency	1050		1850	MHz
Phase Noise @ 10 kHz offset (1 Hz BW)		-100		dBc/Hz
Harmonic Suppression (2nd)		-10		dBc
Spurious Suppression		-75		dBc
Power Output	4	6	8	dBm
Load Impedance		50		Ω
Step Size		1000		kHz
Phase Detector Frequency		32000		kHz
Settling Time		.01		mS
Charge Pump Output Current		940		μ A
Operating Temperature Range	0		70	$^{\circ}$ C
Package Style		PLL-24S1		

Power Supply Requirements	Min	Typ	Max	Units
Supply Voltage 1: PLL (Vcc, nom)		5		Vdc
Supply Voltage 2: VCO (Vcc, nom)		15		Vdc
Supply Current 1: PLL (Icc, typ)		25		mA
Supply Current 2: VCO (Icc, typ)		40		mA

Reference Oscillator Signal	Min	Typ	Max	Units
Frequency		32		MHz
Phase Noise @1 kHz offset		-145		dBc/Hz

Additional Notes

Reference Oscillator Signal: $32\text{ MHz} < f_{\text{osc}} < 250\text{ MHz}$. Frequency Synthesizer: Analog Devices - ADF4156.
Smaller step sizes are possible with smaller PDF. Fractional-N PLL.

LFSuffix = RoHS Compliant. All specifications are subject to change without notice.

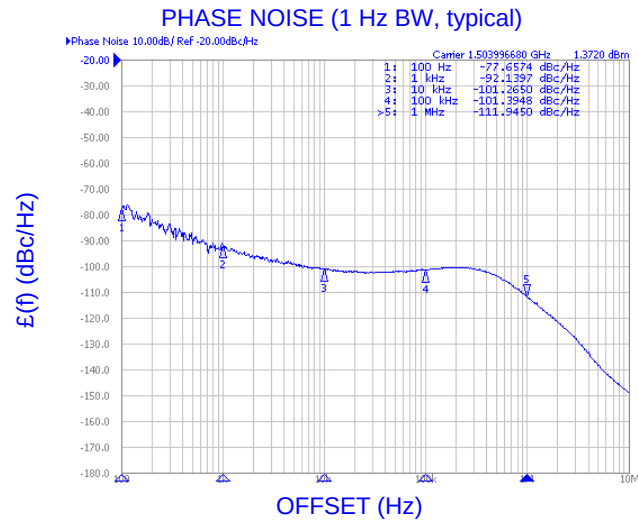
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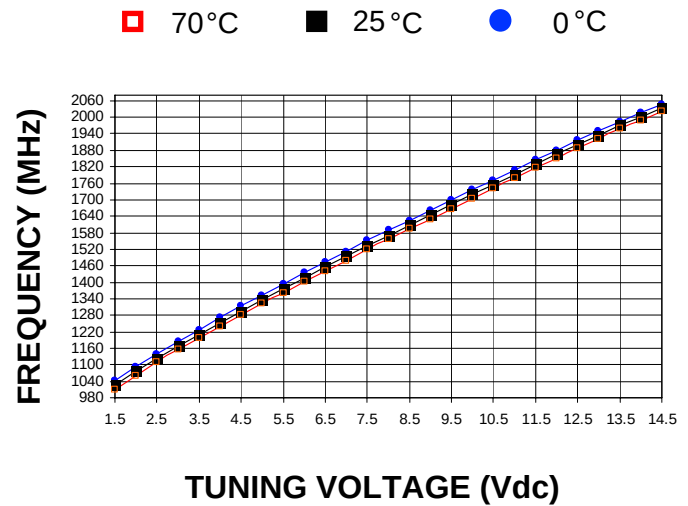
URL: www.zcomm.com | EMAIL: applications@zcomm.com



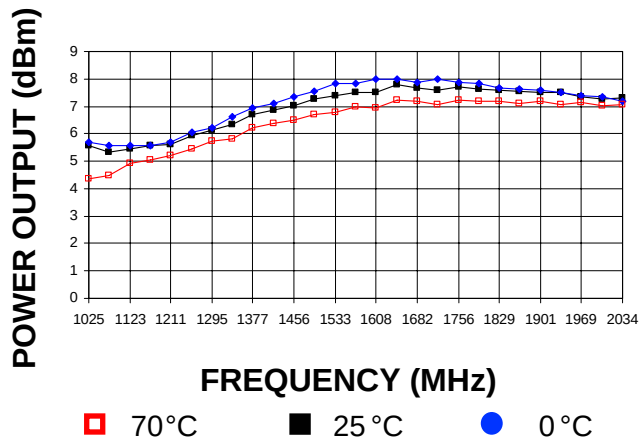
Phase Noise, typ.



Tuning Curve, typ.



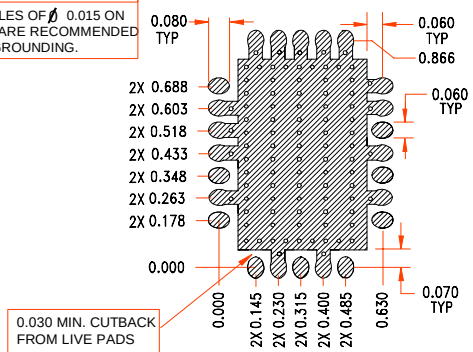
Power Curve, typ.



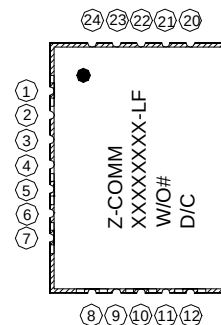
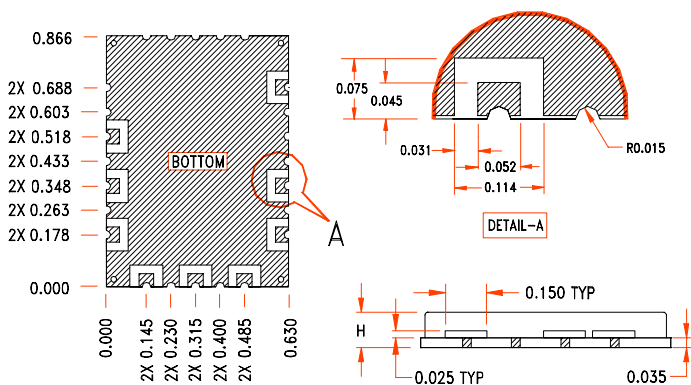
Footprint

RECOMMENDED FOOTPRINT

SEVERAL HOLES OF ϕ 0.015 ON GND. PLANE ARE RECOMMENDED FOR GOOD GROUNDING.



Physical Dimensions



PIN CONFIGURATION

1	RF OUT
5	REF IN
7	CLOCK
8	DATA
10	LOAD ENABLE
12	MUX
13	Vcc1 (PLL)
15	Vcc2 (VCO)
17	N/C
REST	GROUND

PACKAGE	H
PLL-24S1-H	0.220
PLL-24S1	0.140

NOTE: ALL DIMENSIONS ARE IN INCHES
TOL: XXX: +/- 0.010